The FE-I4 Pixel Readout IC

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FE-I4 Design Collaboration

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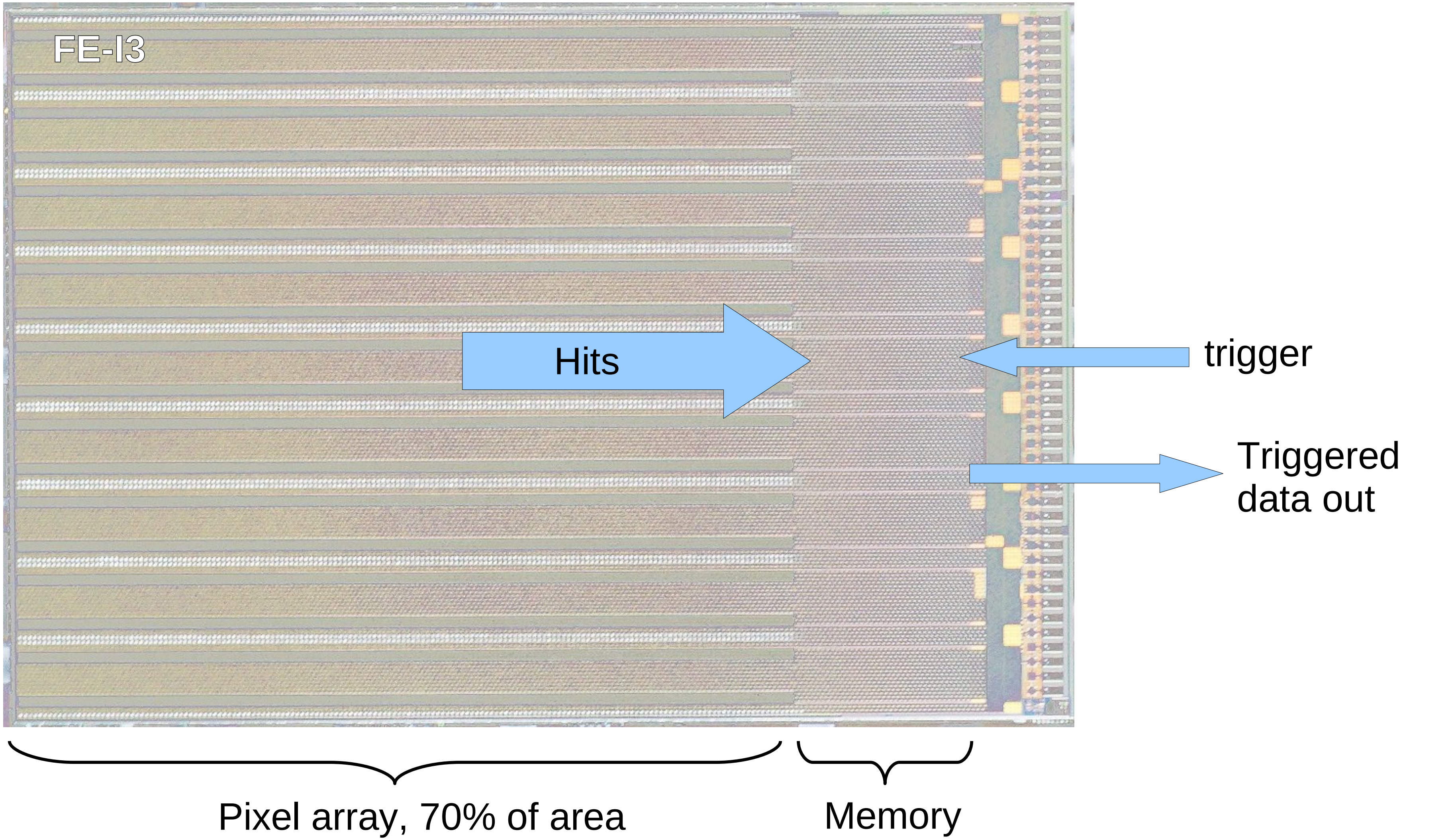
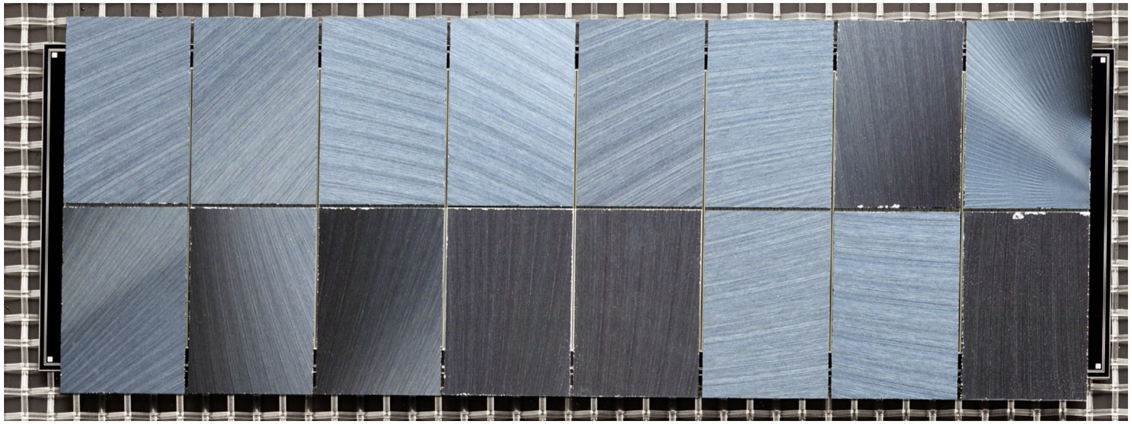
Designers collaborate remotely using the Cliosoft collaboration platform.

Today's ATLAS pixel chip

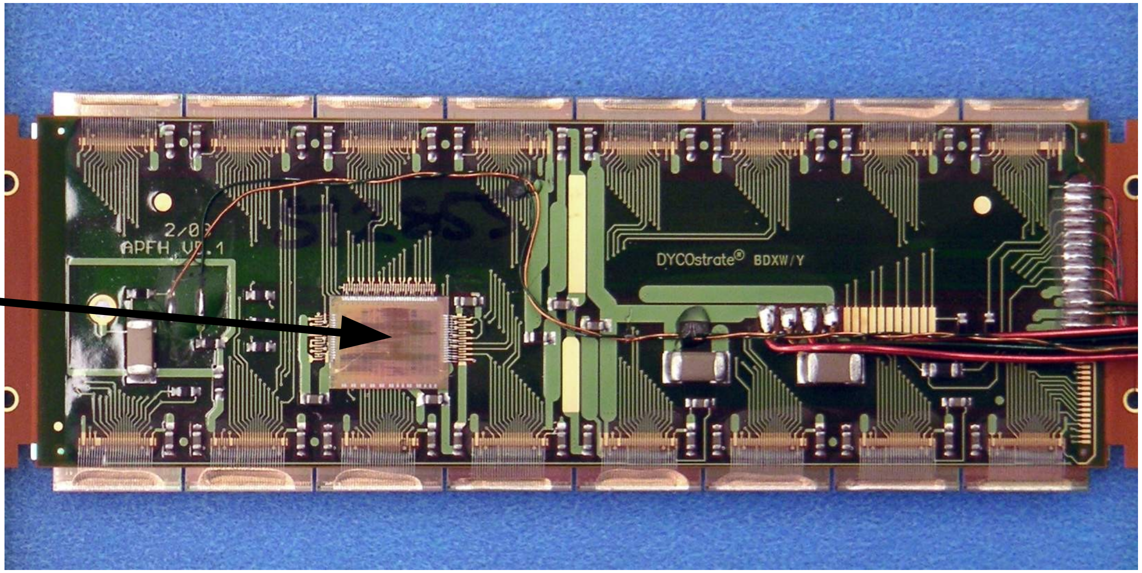


Today's ATLAS module

16 chips on 1 sensor to cover a ~10cm^2 area



Digital module control chip



What would be better?
(a.k.a. FE-I4 specs)

- Much cheaper module manufacture
  (=> chip size as big as possible)
- Greater fraction of the footprint devoted to pixel array
  (=> move the memory inside the array)
- Lower power
  (=> don't move the hits around unless they are triggered)
- Able to take higher hit rate
  (=> store the hits locally and distribute the trigger)
- Still able to resolve the hits at higher rate
  (=> smaller pixels and faster recovery time)
- No need for extra control chip
  (=> significant digital logic blocks on array periphery)

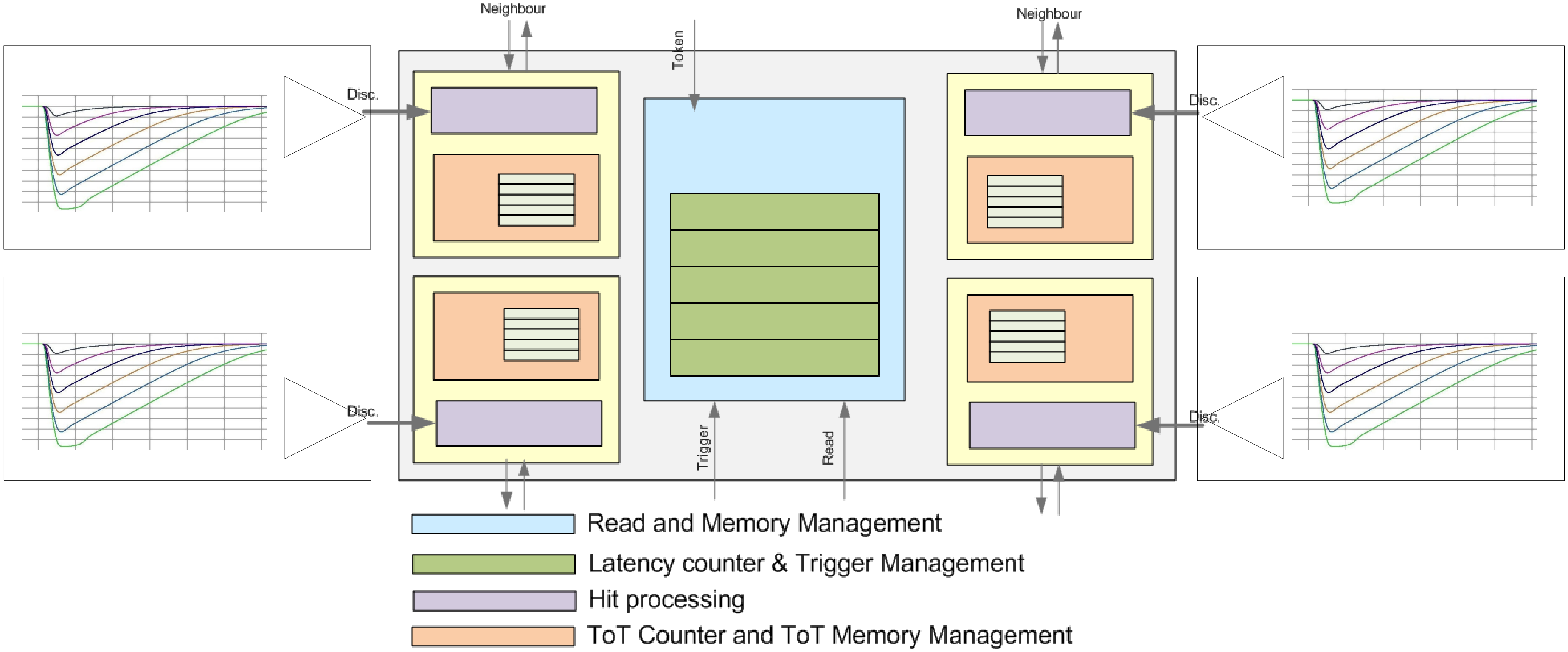
Region architecture

FE-I4 Pixel

- Basic problem is how to reduce the pixel size and at the same time move memory and trigger processing into the pixel
- Move from 250nm CMOS6RF to 130nm CMOS8RF.
- Use linear transistors instead of enclosed layout
  - Any “analog” NMOS (i.e. one that is not a switch) is placed inside a guard ring, but geometry is still linear.
- Digital circuitry (hit memory and logic) in pixel is all synthesized standard cells.
- Is this enough? No
- The final improvement is to group the pixels into units called regions where the trigger processing is shared.
- This helps because hits from charged particles are naturally clustered.
  - If hits were random, with no spatial correlation, it would be less useful

Region

- 4 analog pixels, each ending with a comparator output (ADC function).
- One common digital region synthesized as one block.
- 5-deep TOT value memory for each pixel, but shared trigger latency counters.
- If 1 pixel is hit, 1 counter starts. If 2,3,4 pixels are hit, also only 1 counter starts.
- No region dead time (pixel A hit this crossing and B hit next crossing is OK)



Analog pixel

Design:

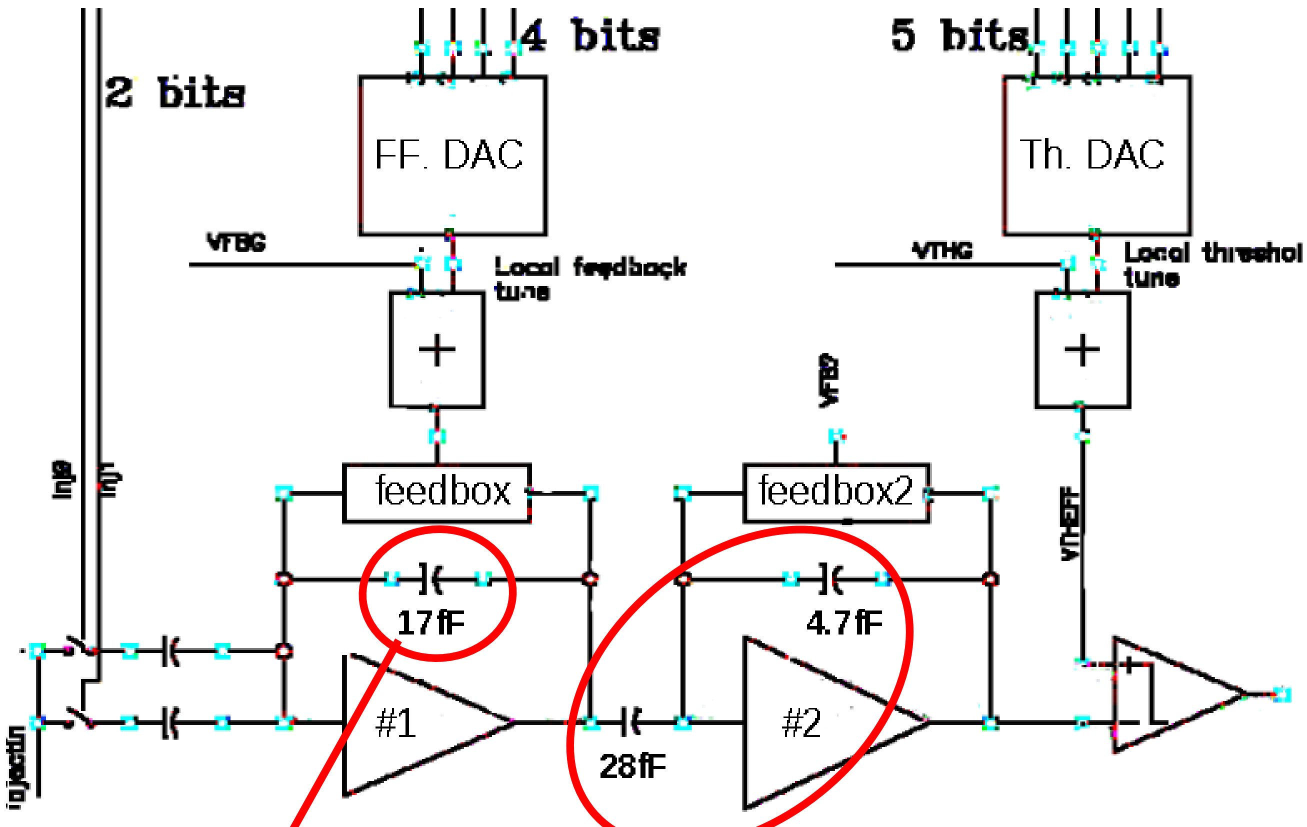
1.2V – 1.5V

5µA – 17µA

Baseline:

10µA @ 1.4V

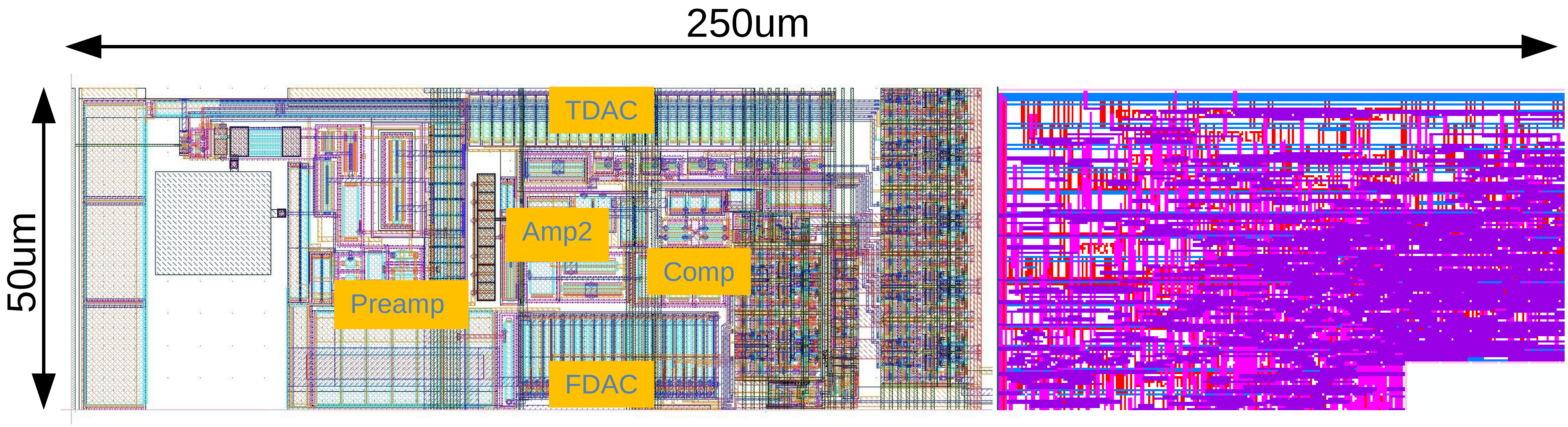
Same as present detector baseline per unit area



~4MIP
dynamic range

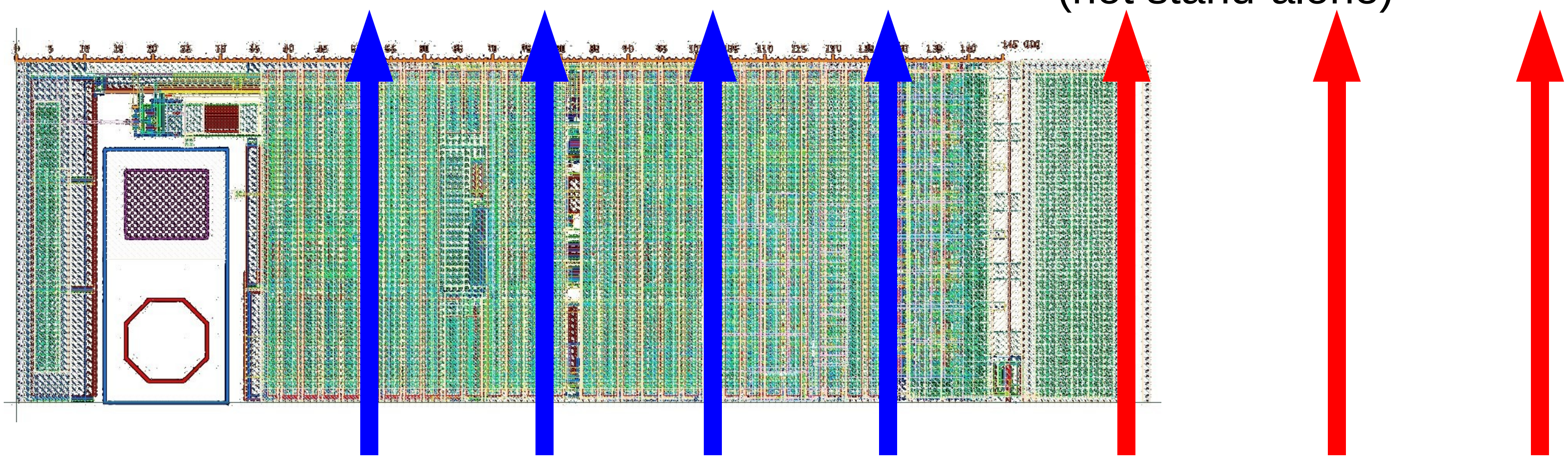
X6
No shaping

FE-I4 Pixel Layout



Custom layout.

Part of synthesized region
(not stand-alone)



Power distribution and shield on top metals. Only vertical - no analog/digital crossing

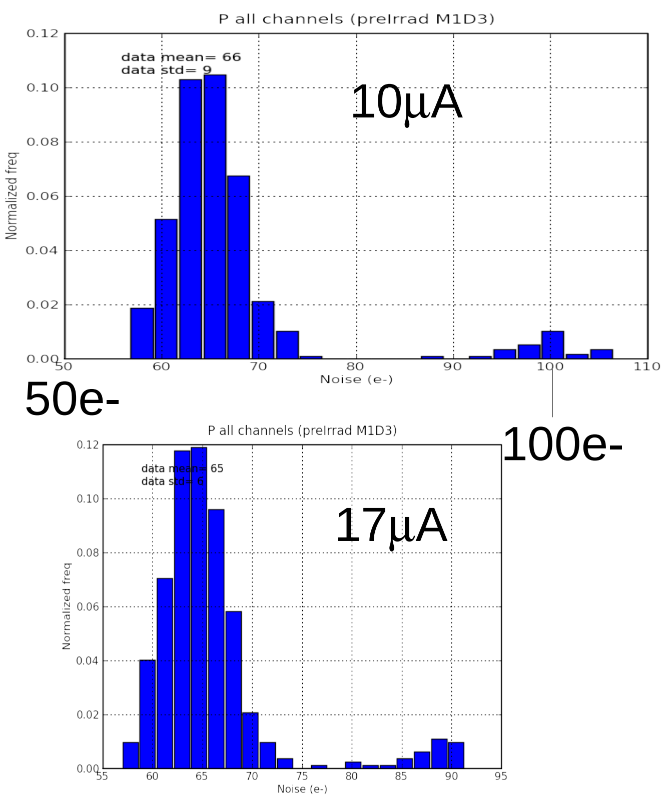
Noise Performance

(measured in pixel array test chip)

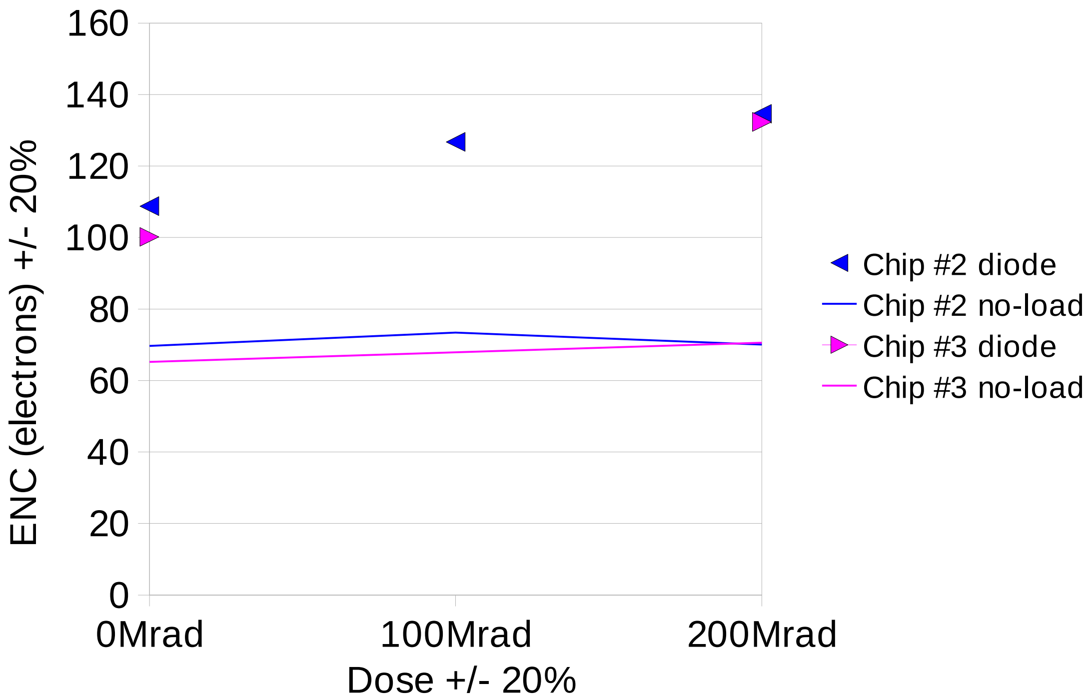
Noise

unloaded

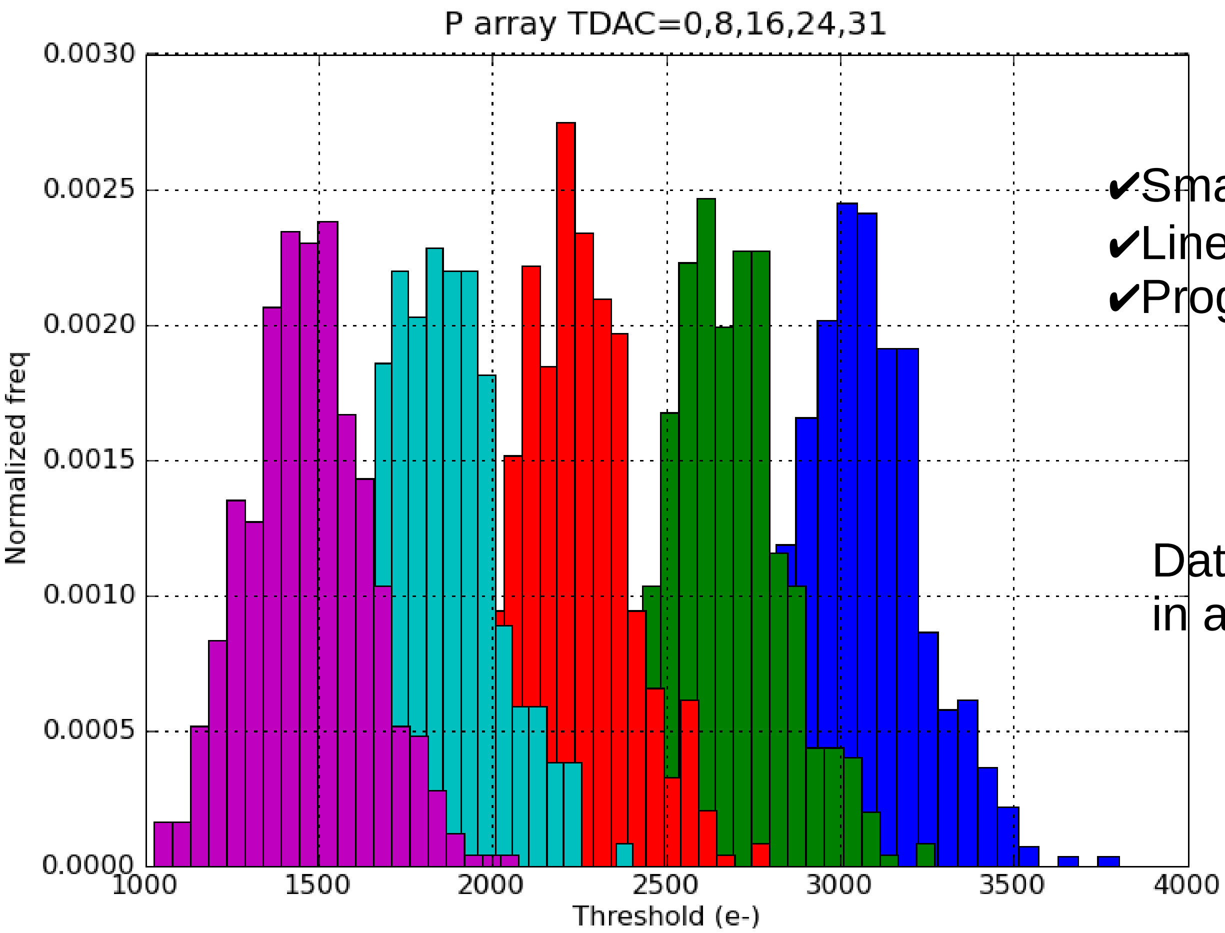
~400fF



Irradiation:
Loaded channels increased ~20%,
But load is a diode!
The load itself changes with radiation
No bump-bonded assemblies yet.



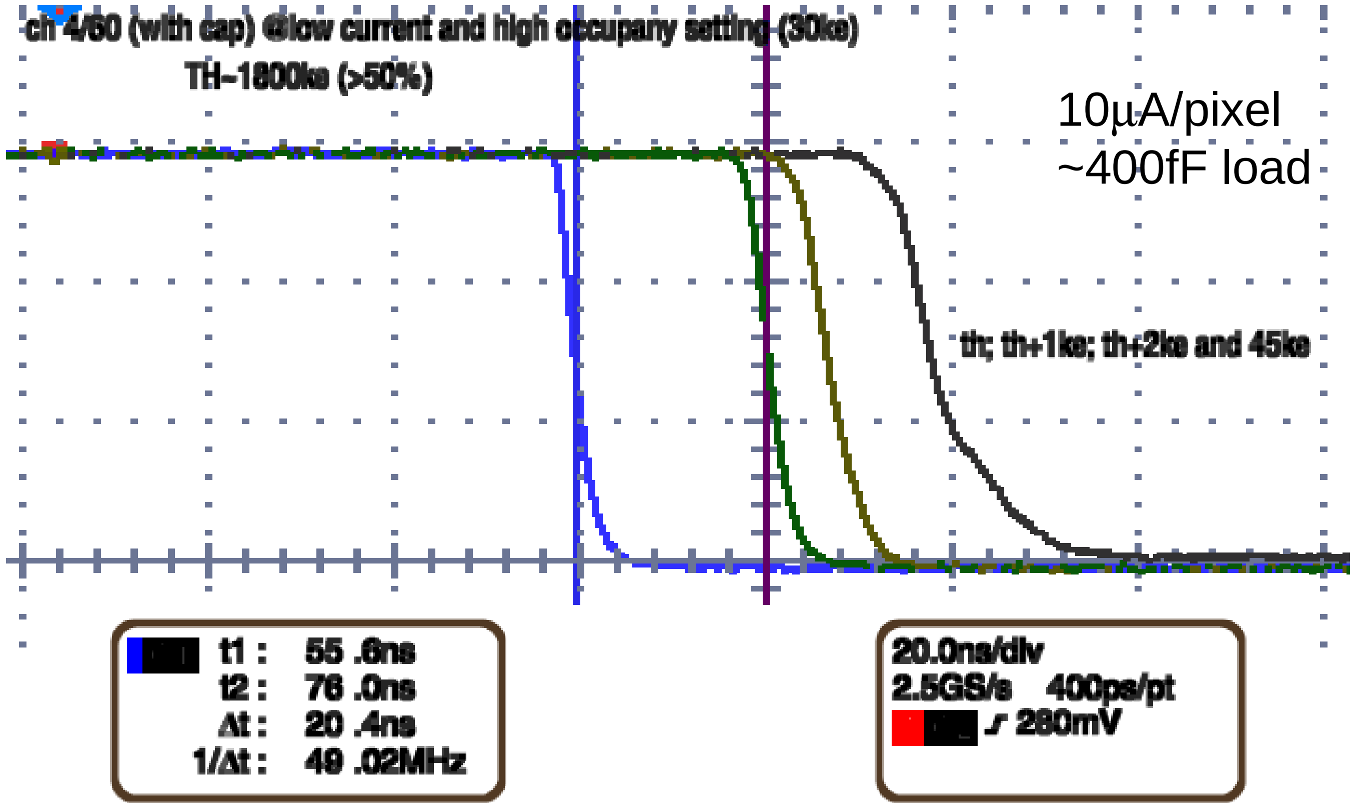
Threshold



- ✔Small dispersion (~200e- σ)
- ✔Linear DAC adjustment
- ✔Programmable step size

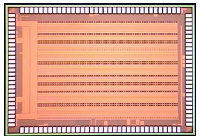
Data from 480 pixels in array test chip

Time-walk

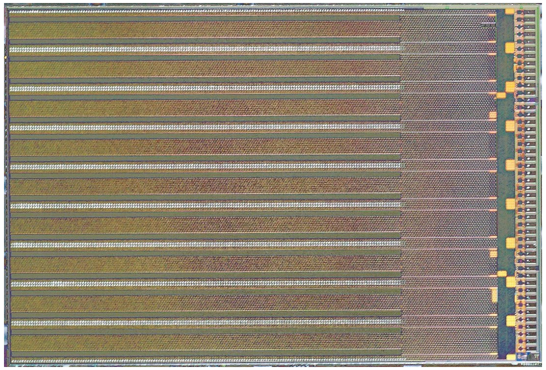


- Can be reduced by increasing analog current
- But there is no need (see later)

Die footprints to same scale

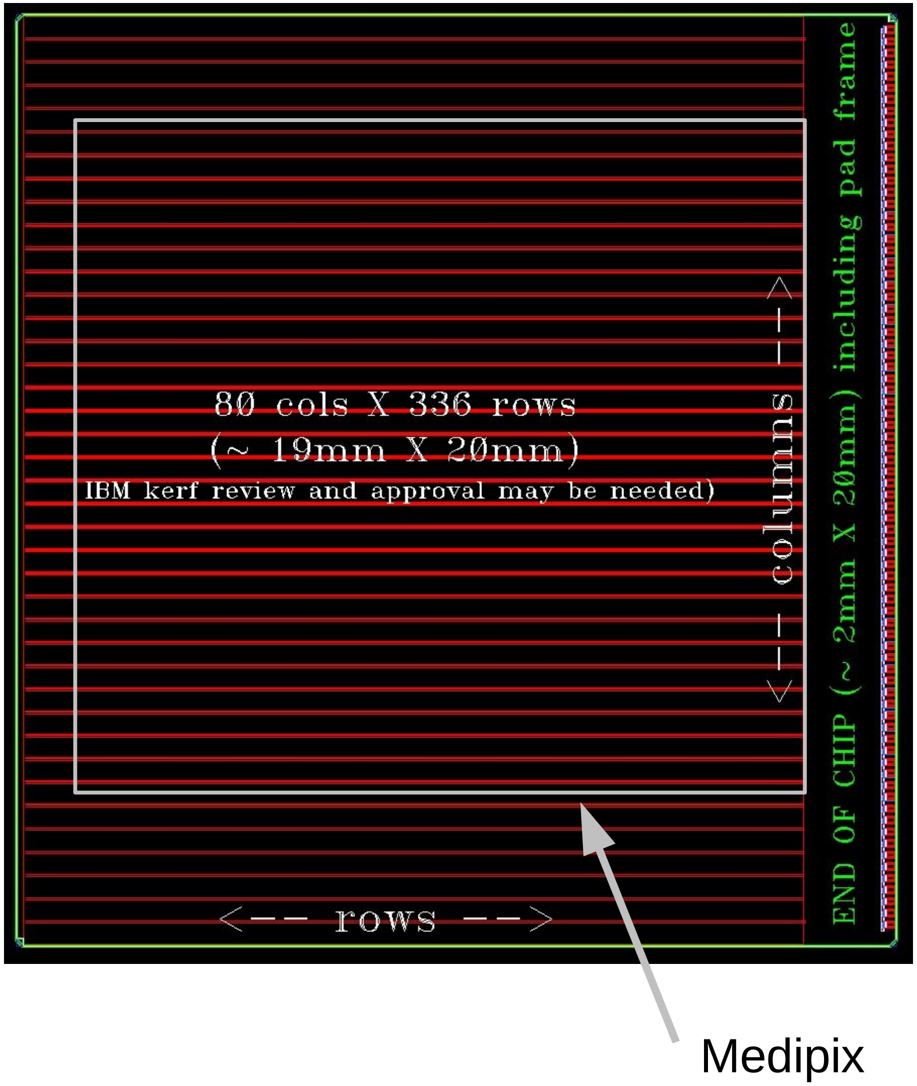


Analog pixel array demonstrator
Fabricated in 2008
Validation of analog performance
and radiation tolerance
(also digital circuit, LVDS, LDO, DC-DC, bias generator, etc.)



FE-I3
(present detector)

FE-I4



FAQ

- Won't such a big chip have zero yield?
- What, you're placing synthesized standard cells next to sensitive amplifiers?!
- Why isn't lower analog performance due to reduced current an issue?
- What will be the minimum threshold for stable operation?
    - Sorry, we are not able to make a quantitative prediction for this.

Yield hardening

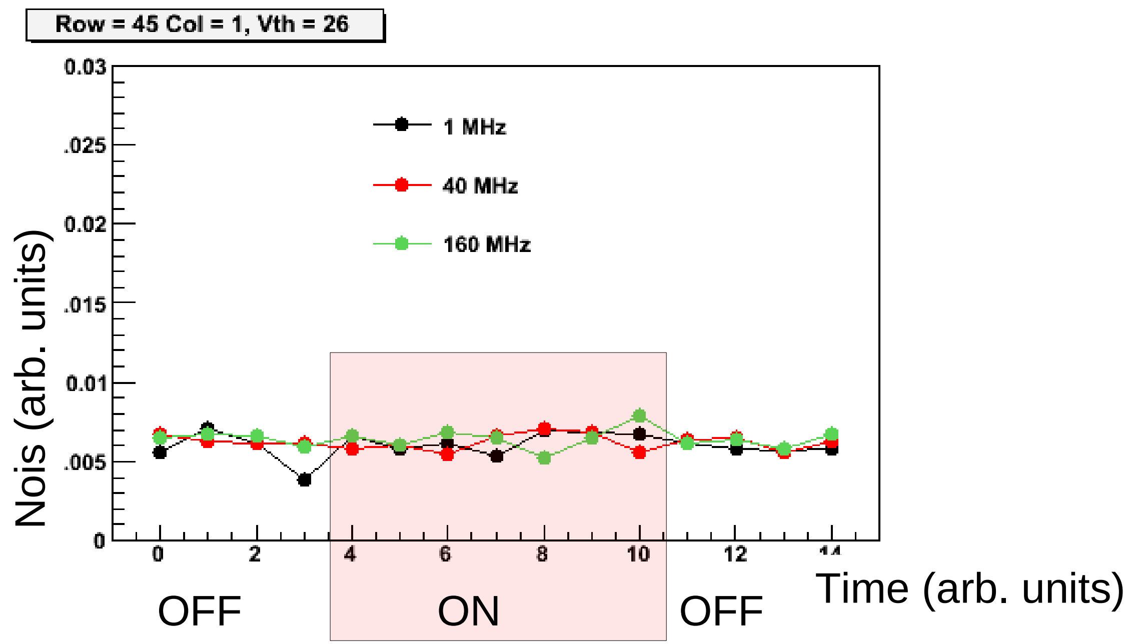
- Critical point: a physics grade pixel chip is NOT a perfect chip.
  - A certain fraction of dead pixels is acceptable
  - For present detector that was 5/2880 at wafer probing
  - “Vulnerable” area of chips << footprint
- Nevertheless, for such a large chip we are combining 2 yield hardening approaches
  - Make probing “part of Fab” (for pixel config. SR & decoder)
    - Use e-fuses to select between 2 SR's at probing
  - Use standard defect tolerant methods requiring no user action
    - All region outputs Hamming coded
    - Read token triple redundant
    - Note SEU not an issue for internal data buses. Do not need to “preserve” redundancy for operation.
- Hope to use Medipix 3 wafer probe results to create a yield model for FE-I4

Substrate Coupling

- Standard cells hard-wire substrate to digital G.
  - Bad for sensitive analog circuits on same substrate.
- But nevertheless would like to take advantage of “canned” digital design flow.
- In this era of system-on-a-chip, we can't be the only ones with this problem!
- Plan to use new feature offered in CMOS8RF called T3 isolation
  - Basically a big N-well (100μm x anything) where a synthesized block can be placed.
  - Seems tailored to “our” particular problem.
  - Very small effect on circuit area.

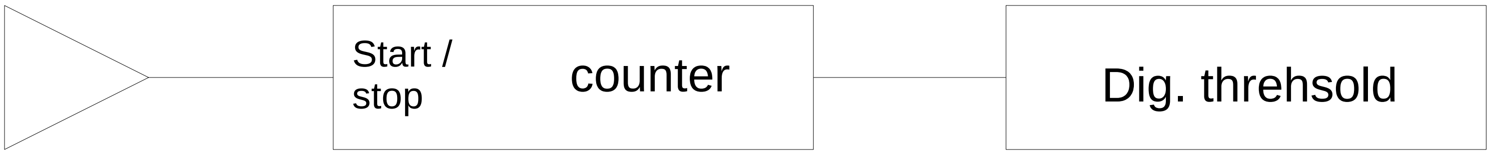
Substrate coupling tests

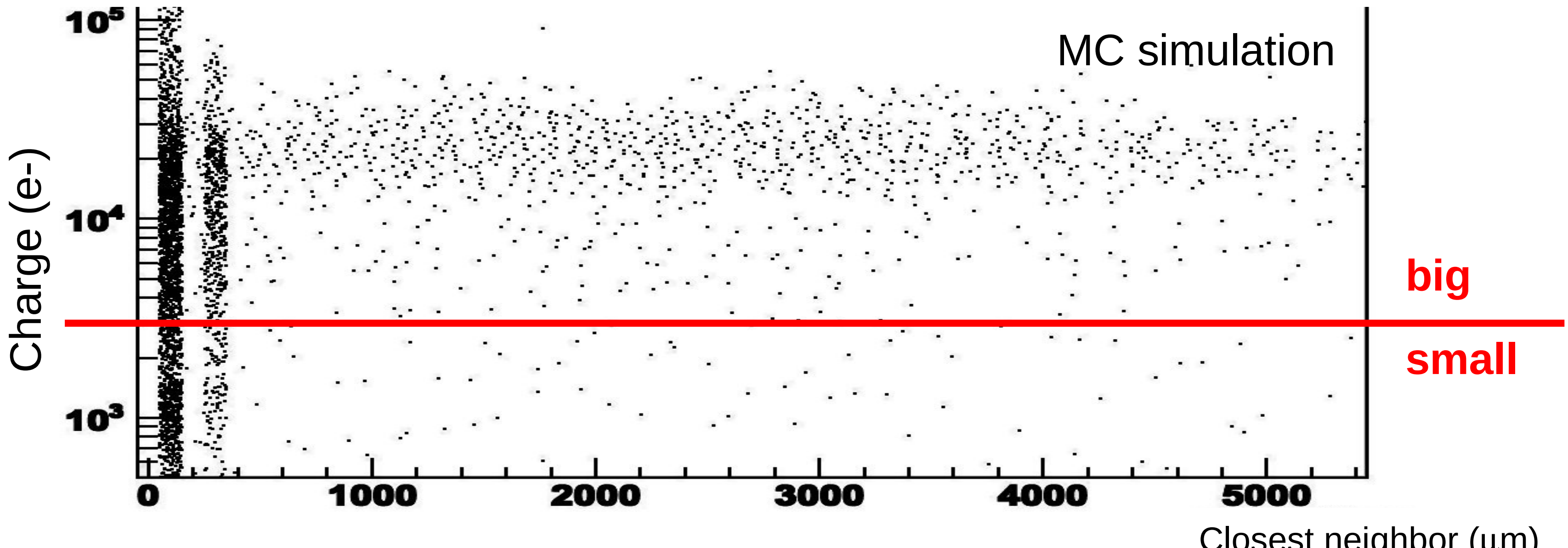
- Have tried to noise coupling from a synthesized standard cell block to analog pixels in 2008 array test chip
    - No isolation was used here
- This does not prove anything, but suggests potential substrate coupling may not be very large.



Hit association

- Recall claim “higher current to improve time-walk not needed”
- Because we use a digital threshold with association of “small hits” by proximity, not time.
  - Large hits are in time
  - Small hits are close to large hits





Other chip features prototyped and tested

- SEU registers- custom layout
- Shunt-LDO regulators for power conditioning and/or serial power implementation
- X2 Charge pump DC-DC converter
- Clock multiplier for up to 320Mb/s output from 40MHz input clock.
- LVDS compatible I/O
- Scan chains for testing digital circuitry
- Total dose (to 200MRad) and SEU radiation testing
- Detailed simulations of digital power consumption in array
  - (<10uA /pixel @ 1.2V)

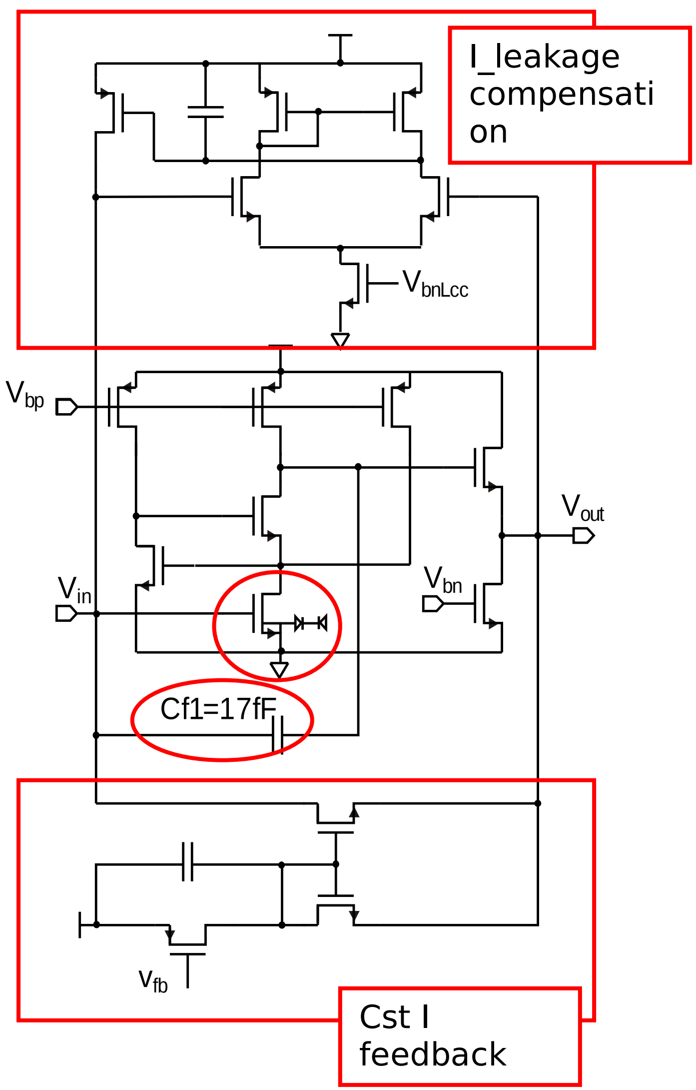
Conclusions

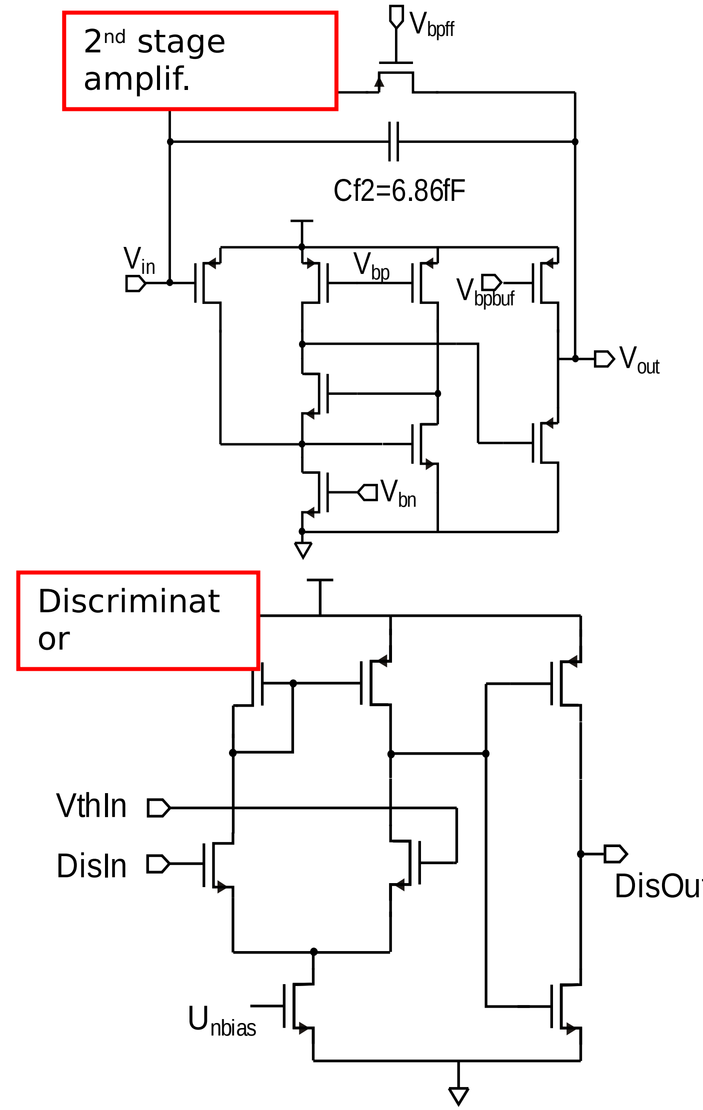
- FE-I4 blocks are technology choices defined.
- Will be the largest HEP pixel chip to date
  - Large reduction of module assembly cost
  - Expect yield of physics grade chips to be reasonable,
  - But additionally yield hardening the design of most blocks.
- Basic performance validated with small prototypes.
- Integration of a full size chip started
  - Submission planned this Fall (date not yet fixed)
- Will use synthesized standard cell layouts for all digital elements, with T3 isolation to keep substrate clean
- Distributed design collaboration approach is working very well.

BACKUP

Analog pixel

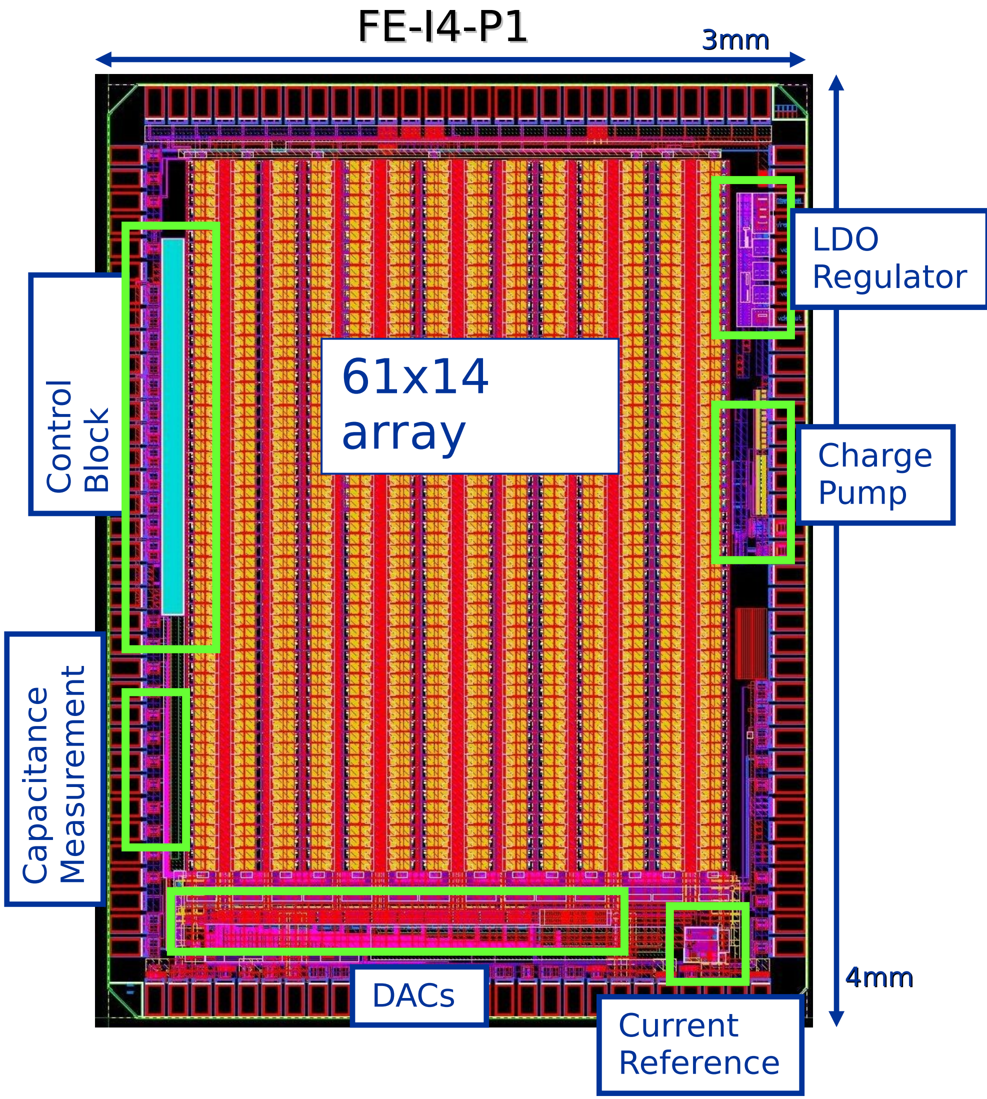
preamp

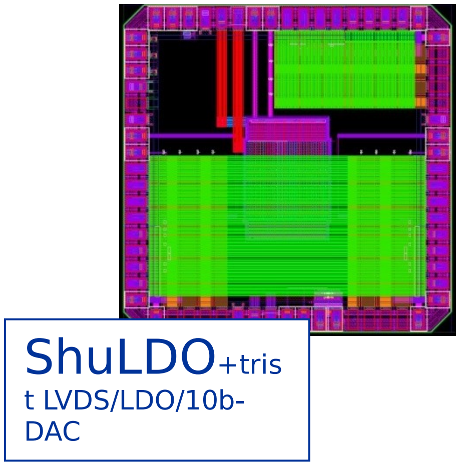




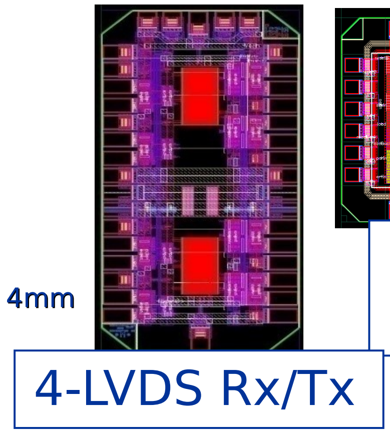
FE-I4 test chips

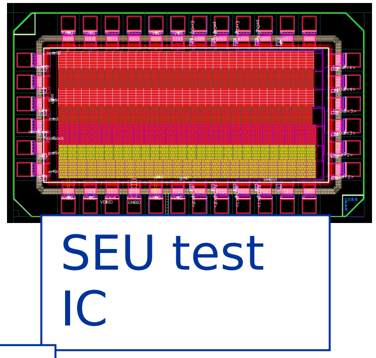
Also ported to Chartered in 2009



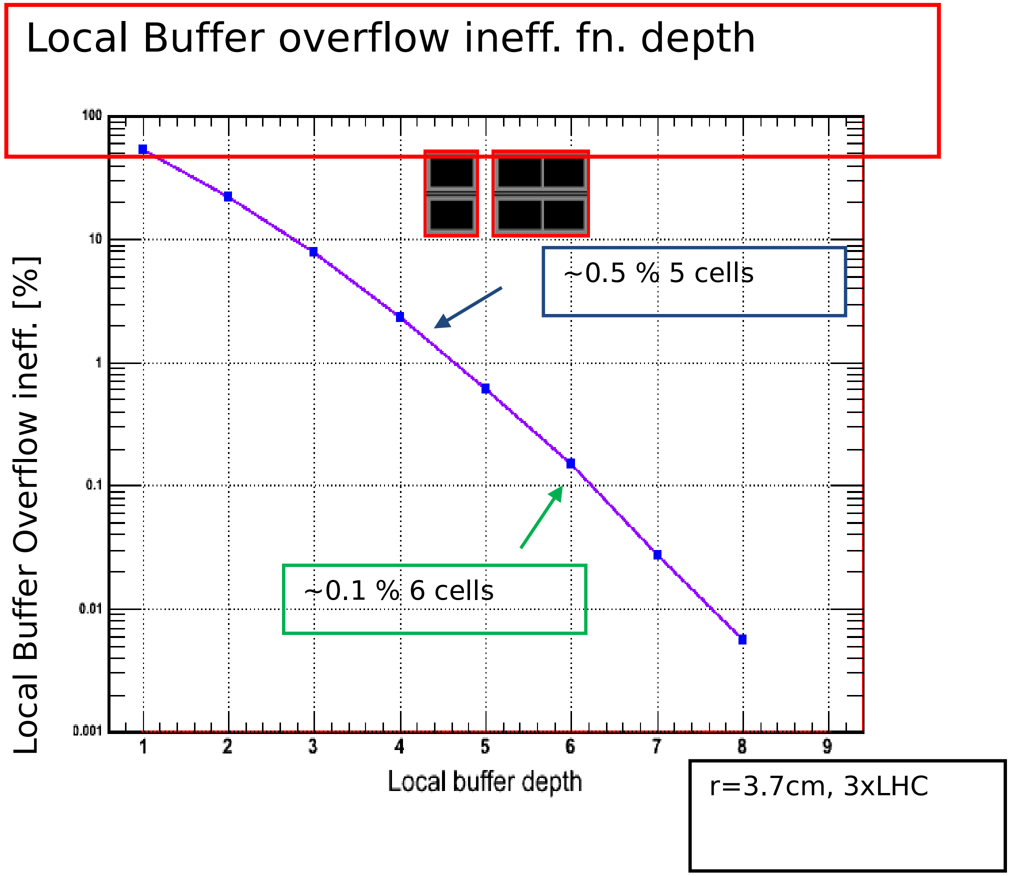


Clock multiplier





Functional simulations (example)



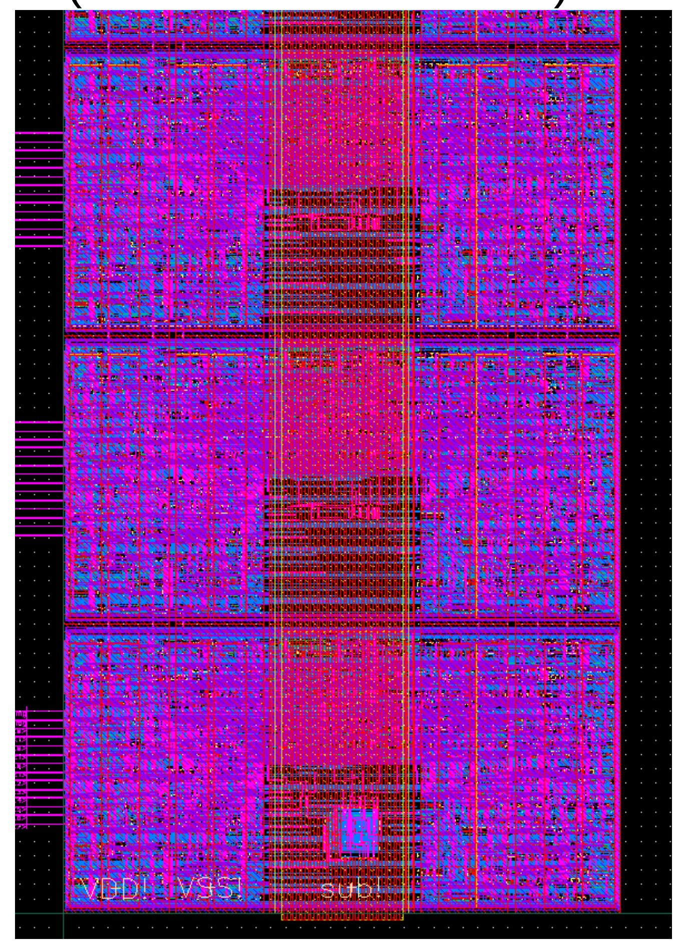
Digital power

Average for 4-pixel region. IBL occupancy

Simulation type	Power (avg) [uW]
ETS[1]	42.28
Spectre[2]	25.19
Ultarasim(s)[2]	24.69
Ultarasim(a) [2]	24.73
Ultarasim(ms) [2]	35.12
HSIM[1]	27.64
HSIM[2]	30.98

@1.2V

Digital column pair layout
(30K transistors shown)



300um slice

Parasitic extraction done
width [1]PEX